***Semester : 5th***

***(Regular&Back)***

***COA & CS-3005/CS-505***

***Branch (s) : CSE, IT, DD M. Tech, DD*** MBA

**kiitlogo AUTUMN END SEMESTER EXAMINATION-2015**

**COMPUTER ORGANIZATION AND ARCHITECTURE**

**[ CS-3005/CS-505 ]**

**Full Marks: 60 Time: 3 Hours**

***Answer any six questions including question No.1 which is compulsory.***

***The figures in the margin indicate full marks.***

***Candidates are required to give their answers in their own words as far as practicable and***

***all parts of a question should be answered at one place only.***

(Instruction format: Opcode src2, src1/dest)

Q No: Contents Marks

1. Short Questions [ 2 ×10]
2. Registers R1 and R2 of a computer contain the decimal values 1200 and 4600. What is the effective address of the memory operand in each of the following instructions?

LOAD 50(R1), R5

STORE R5, 20(R1,R2)

1. Consider a computer that has a byte-addressable memory organized in 32-bit words according to the big-endian scheme. A program reads ASCII characters entered at a keyboard and stores them in successive byte locations, starting at location 1000. Show the contents of the two memory words at locations 1000 and 1004 after the name "Johnson" has been entered.
2. A two word instruction is stored in a location A. The operand part of instruction holds B. If the addressing mode is relative, the operand is available in which location?
3. A relative mode branch type of instruction is stored in memory at an address equivalent to decimal 850. The branch is made to an address equivalent to decimal 300. What should be the value of the relative address field of the instruction (in decimal)?
4. What is stack frame? Give an example of stack frame for nested subroutine.
5. The computer has an instruction set consisting of 175 different operations. The memory unit has 32 bits per word. Each instruction is stored in one word of memory and allows two addresses ( one register address and one memory address ). If there are 40 registers then what is the maximum allowable size for memory?
6. How many RAM chips of size 128K × 16 are required to provide a capacity of main memory equal to 4M × 32 ?
7. A CPU has 30-bit memory address and 128K bytes of cache memory. The cache is organized as a 4-way set associative cache with a block size of 16 bytes. What is the number of sets?
8. Throughput of pipeline and non-pipeline system are 8 and 2 MIPS. Let the pipeline operating with 80% efficiency. What will be the number of stages in pipeline?
9. Write the IEEE 754 single precision floating point represent of the decimal number 12.25.
10. [ 4 × 2]
11. What is virtual memory? Explain the address translation mechanism of virtual memory using TLB.
12. A computer has 40 bit instruction. It uses one register operand and one memory operand. There are 128 general purpose registers and 256M bytes of RAM. How many different operations the computer can perform if the indirect bit (mode) is used as the part of the operation code? If there are 'n' two address operations which uses both register and memory, then how many one address operations (which use only memory) are possible.
13. [ 4 × 2]
14. Write an assembly program to read a line of characters typed at a keyboard and send them out to a display device. Assume that bit 'b2' in registers INSTATUS and OUTSTATUS corresponds to SIN and SOUT respectively.
15. What is pipeline hazard? Explain types of hazards and write the solutions for data hazard.
16. [ 4 × 2]
17. An instruction is stored at location 600 with its address field at location 601. The address field has the value 100. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is direct, immediate, relative, register indirect, and index with R1 as the index register.
18. Multiply two numbers (-9) × (-13) = + 117 by using Booth's Algorithm. Give the flow table of the multiplication.
19. [ 4 × 2]
20. Write the micro routine for the following instruction:

ADD R1,(R2)

1. Draw and explain 3-bus CPU organization and write the control signals to execute following instruction using same organization

ADD R1,R2,(R3)

1. [ 4 × 2]
2. What is content addressable memory? Explain the working principle and match logic of content addressable memory with suitable diagrams. How it is different from RAM?
3. Consider a two level memory system such that the level-1 having hit ratio 70%. The level-1 memory is 10 times faster than level-2 memory. The average access time of level-1 memory is 50ns. If the average access time of level-2 memory is changed or increased by 20% of 50ns. Compute the followings.

( i ) What is the access time of level-1 memory?

( ii )What is the new hit ratio?

( iii )What is the percentage of change in hit ratio?

1. [ 4 × 2]
2. Explain the importance of interrupt vector in I/O Processing? What is daisy chain method for handling simultaneous interrupt request.
3. There are two instruction pipeline A and B. Pipeline A has 9 stages with uniform stage delay of 2 ns. Pipeline B has 5 stages and stage delays are 2ns, 4ns, 3ns, 2ns, and 2ns. Buffer overhead is 1ns for each case. How much time is saved while executing 100 instructions by choosing pipeline A instead of B?
4. Write Short Notes ( Answer any Two): [ 4 × 2]
5. Von-Neumann Architecture VS Harvard Architecture.
6. Hardwired control unit VS Microprogrammed Control Unit
7. Memory mapped I/O VS I/O mapped I/O
8. RISC VS CISC

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Moderator……………………….